WHAT IS CLAIMED IS

1. A semiconductor device which receives addresses in synchronism with a clock signal and receives data in synchronism with a strobe signal, said semiconductor device comprising:

address-latch circuits which latches the addresses;

a first control circuit which selects one of said address-latch circuits in sequence in response to the clock signal, and controls the selected one of said address-latch circuits to latch a corresponding one of the addresses in response to the clock signal; and

a second control circuit which selects one of said address-latch circuits in sequence in response to the strobe signal, and controls the selected one of said address-latch circuits to output a corresponding one of the addresses in response to the strobe signal.

2. The semiconductor device as claimed in claim 1, further comprising data-latch circuits, each of which latches a corresponding datum of the data in synchronism with the strobe signal, and outputs the corresponding datum of the data in synchronism with the strobe signal.

3. The semiconductor device as claimed in

claim 2, wherein said data-latch circuits operate in response to a write-enable signal which is generated in response to a write command to said semiconductor device.

4. The semiconductor device as claimed in claim 3, wherein the write-enable signal controls said first control circuit and said second control circuit to operate for a predetermined time period after receiving the write command.

5. The semiconductor device as claimed in claim 1, wherein said first control circuit includes a first frequency divider configured to divide a frequency of the clock signal, and selects one of said address-latch circuits in sequence by using the frequency-divided clock signal from said first frequency divider, and said second control circuit includes a second frequency divider configured to divide a frequency of the strobe signal, and selects one of said address-latch circuits in sequence by using the frequency-divided clock signal from said second frequency divider.

6. The semiconductor device as claimed in claim 1, further comprising:

an increment-latch circuit which latches one of the addresses in synchronism with the clock signal;

and

an address-generation circuit which increments the one of the addresses latched by said increment-latch circuit by 1, and supplies the incremented address to said address-latch circuits,

wherein each of said address-latch circuits configured so as to be capable of selecting the corresponding one of the addresses externally provided or the incremented address supplied from said address-generation circuit for the latching operation thereof.

7. The semiconductor device as claimed in claim 2, wherein said data-latch circuit comprises:

a first data-latch circuit which latches a corresponding datum of the data in synchronism with a rising edge of the strobe signal; and

a second data-latch circuit which latches a corresponding datum of the data in synchronism with a falling edge of the strobe signal.

8. A semiconductor device which receives addresses in synchronism with a clock signal and receives data in synchronism with a strobe signal, said semiconductor device comprising:

data-latch circuits;

a first control circuit which selects one of said data-latch circuits in sequence in response to the strobe signal, and controls the selected one of said data-latch circuits to latch a corresponding datum of the data in response to the strobe signal; and

a second control circuit which selects one of said data-latch circuits in sequence in response to the clock signal, and controls the selected one of said data-latch circuits to output a corresponding datum of the data in response to the clock signal.

9. The semiconductor device as claimed in claim 8, further comprising an address-latch circuit which latches the addresses in sequence in synchronism with the clock signal, and outputs the addresses in synchronism with the clock signal.

10. The semiconductor device as claimed in claim 8, wherein said address-latch circuit operates in response to a write-enable signal which is generated in response to a write command to said semiconductor device.

11. The semiconductor device as claimed in claim 10, wherein the write-enable signal controls said first control circuit and said second control circuit to operate for a predetermined time period after receiving the write command.

12. The semiconductor device as claimed in

claim 8, wherein said first control circuit includes a first frequency divider configured to divide a frequency of the strobe signal, and selects one of said data-latch circuits in sequence by using the frequency-divided strobe signal from said first frequency divider, and said second control circuit includes a second frequency divider configured to divide a frequency of the clock signal, and selects one of said data-latch circuits in sequence by using the frequency-divided clock signal from said second frequency divider.

13. The semiconductor device as claimed in claim 9, further comprising

an address-generation circuit which increments one of the addresses latched by said address-latch circuit, and supplies the incremented address to said address-latch circuit,

wherein said address-latch circuit is configured so as to be capable of selecting the addresses externally provided or the incremented address supplied from said address-generation circuit for the latching operation thereof.

14. The semiconductor device as claimed in claim 8, wherein each of said data-latch circuits includes:

a first latch which latches a corresponding datum of the data in synchronism with a rising edge of the strobe signal; and

a second latch which latches a corresponding

datum of the data in synchronism with a falling edge of the strobe signal.

15. The semiconductor device as claimed in claim 9, wherein said address-latch circuit includes a delay circuit which delays output timings of the addresses by a predetermined number of cycles of the clock signal.

16. The semiconductor device as claimed in claim 1, further comprising an address buffer, wherein said address-latch circuits supply the addresses to said address buffer without a clock-cycle delay during a read operation.

17. The semiconductor device as claimed in claim 9, further comprising an address buffer, wherein said address-latch circuit supplies the addresses to said address buffer without a clock-cycle delay during a read operation.

18. A memory circuit, comprising:

an address-input circuit which latches address signals in response to a clock signal, and outputs the address signals in response to a timing

signal;

a data-input circuit which latches data signals in response to a strobe signal, and outputs the data signals in response to the timing signal; and

an internal circuit which writes the data signals supplied from the data-input circuit in memory cells indicated by the address signals supplied from the address-input circuit.

19. The memory circuit as claimed in claim 18, wherein said timing signal is responsive to the strobe signal.

20. The memory circuit as claimed in claim 18, wherein said timing signal is responsive to the clock signal.

21. The memory circuit as claimed in claim 18, wherein the strobe signal has a cycle identical to that of the clock signal, and a first timing of a first rising edge of the strobe signal is different from a second timing of a corresponding rising edge of the clock signal.

22. The memory circuit as claimed in claim

21, wherein the first timing is later than the second timing with a timing gap therebetween being shorter than one cycle of the clock signal.

23. The memory circuit as claimed in claim 18, wherein said data-input circuit latches the data signals in synchronism with rising edges and falling edges of the strobe signal.

24. The memory circuit as claimed in claim 19, wherein the address-input circuit includes:

a first latch circuit which latches the address signal in response to a first rising edge of the clock signal, and outputs the address signal in response to the timing signal; and

a second latch circuit, connected in parallel to the first latch circuit, which latches next address signal in response to a next rising edge of the clock signal, and outputs the next address signal in response to the timing signal.

25. The memory circuit as claimed in claim 24, wherein the address-input circuit outputs the address signal prior to outputting the next address signal.

26. The memory circuit as claimed in claim 19, further comprising:

a decode circuit which receives the address signal from the address-input circuit, and decodes the address signal in response to a first activation signal; and

a write amplifier which receives the data signal from the data-input circuit, and amplifies the data signal in response to a second activation signal in a data-write mode,

wherein both of the first and second activation signals are responsive to the strobe signal in the data-write mode.

27. The memory circuit as claimed in claim 26, wherein in a data-read mode, the first activation signal is responsive to the clock signal, and the second activation signal is in a deactivated state.

28. The memory circuit as claimed in claim 20, wherein said data-input circuit includes:

a first data-input circuit which latches the data signals in sequence in response to a first rising edge and a first falling edge of the strobe signal, and outputs the data signals in parallel in response to the timing signal; and

a second data-input circuit, connected in parallel to the first data-input circuit, which latches next data signals in sequence in response to a next rising edge and a next falling edge of the strobe signal, and outputs the next data signals in parallel

in response to the timing signal.

29. The memory circuit as claimed in claim 20, wherein said data-input circuit includes a first data-input circuit which latches the data signals in sequence in response to a rising edge and a falling edge of the strobe signal, and outputs the data signals in parallel in response to the timing signal.

30. The memory circuit as claimed in claim 29, wherein said first data-input circuit latches next data signals after outputting the data signals.

31. The memory circuit as claimed in claim 28, wherein said data-input circuit outputs the data signals prior to outputting the next data signals.

32. The memory circuit as claimed in claim 20, wherein said address-input circuit includes a shift register which operates in response to the clock signal.

33. The memory circuit as claimed in claim 19, wherein said address-input circuit includes a shift register which operates in response to the clock signal.

34. A method of writing data in the memory circuit of claim 33, comprising a step of adjusting an input timing of the strobe signal relative to the clock signal such that said shift register stores two addresses at a time when the data-input circuit outputs the data signals.

35. The memory circuit as claimed in claim 20, further comprising:

a decode circuit which receives the address signal from the address-input circuit, and decodes the address signal in response to a first activation signal; and

a write amplifier which receives the data signal from the data-input circuit, and amplifies the data signal in response to a second activation signal in a data-write mode,

wherein both of the first and second activation signals are responsive to the clock signal in the data-write mode.

36. The memory circuit as claimed in claim 35, wherein in a data-read mode, the first activation

signal is responsive to the clock signal, and the second activation signal is in a deactivated state.

37. The memory circuit as claimed in claim 26, wherein in the data-write mode, the first activation signal activates said decode circuit after said address-input circuit outputs the address signals, and the second activation signal activates said write amplifier after said data-input circuit outputs the data signals.

38. The memory circuit as claimed in claim 35, wherein in the data-write mode, the first activation signal activates said decode circuit after said address-input circuit outputs the address signals, and the second activation signal activates said write amplifier after said data-input circuit outputs the data signals.

39. The memory circuit as claimed in claim 32, wherein said shift register delays the address signals by 1.5 clock cycles of the clock signal.

40. The memory circuit as claimed in claim 18, wherein a timing at which said address-input

circuit outputs the address signals is concurrent with a timing at which said data-input circuit outputs the data signals corresponding to the address signals.

41. The memory circuit as claimed in claim 32, further comprising a bypass circuit provided in parallel to said shift register, wherein the address signals pass through the bypass circuit and bypass said shift register in a data-read mode.

42. The memory circuit as claimed in claim 33, further comprising a bypass circuit provided in parallel to said shift register, wherein the address signals pass through the bypass circuit and bypass said shift register in a data-read mode.